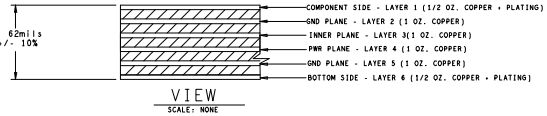
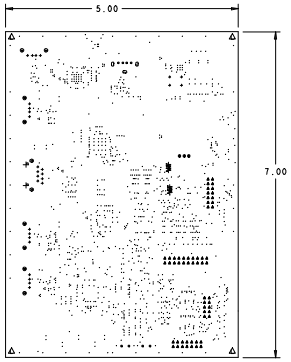
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



VIEW
SCALE: NONE



GOOGLE Inc
SERVO-V2
180-10010-04

DRILL CHART: TOP to BOTTOM				
ALL UNITS ARE IN MILS				
FIGURE	SIZE	TOLERANCE	PLATED	QTY
·	8.0	+3.0/-8.0	PLATED	1291
	12.0	+3.0/-12.0	PLATED	16
+	36.0	+3.0/-3.0	PLATED	4
+	43.0	+3.0/-3.0	PLATED	28
+	47.24	+3.0/-3.0	PLATED	58
+	51.0	+3.0/-3.0	PLATED	3
+	66.93	+3.0/-3.0	PLATED	2
+	90.94	+3.0/-3.0	PLATED	8
△	157.48	+3.0/-3.0	PLATED	4
·	35.83	+3.0/-3.0	NON-PLATED	4
+	127.95	+3.0/-3.0	NON-PLATED	2
⊕	90.55x51.18	+3.94/-3.94	PLATED	2
⊕	90.55x51.18	+3.94/-3.94	PLATED	1

NOTES; Unless otherwise specified

1. General Requirement:
   a. Board shall be built per IPC-A-600 and IPC-6012, class II, latest revision.
   b. Board shall be electrically tested per current revision of IPC 6012 and IPC 9252 class II. Completed electrical test Boards must be marked in permanent non-conductive ink next to supplier UL recognition mark.
   c. Configuration of the printed circuit board not specifically dimensioned on the drawing shall be controlled by the gerber data.
   d. Bow and Twist: shall not exceed .007" per inch.
   e. Fabrication Tolerances; end product trace widths and lands shall not vary more than the smaller of .001" or 20% of the trace width from the gerber data.
   f. PCB fabrication process and materials must be compliant with the Hazadous Substances (RoHS) Directive and compatible with Pb Free assembly process.
   g. Theiving is allowed on all layers with 0.050" squares on 0.100" pitch and 0.100" min away from any designed features (i.e. vias, pads, traces, etc.).
2. Control Impedance;
   Single Ended;
   ~~a. 7.17 mil line on internal layers to be controlled to 37 Ohm, +/- 13%~~
   ~~b. 7.17 mil line on external layers to be controlled to 37 Ohm, +/- 13%~~

   Edge-Coupled Differential:
   e. 4.75mil line with 5.25mil gap on internal layers to be controlled to 90 Ohm, +/- 10%
   f. 4.75mil line with 5.25mil gap on external layers to be controlled to 90 Ohm, +/- 10%
3. Material;
   a. Glass epoxy, natural color, laminated ?????????? with Tg of ???C minimum. The final thickness measured over plating to be 062 mil, +/- 10%.
4. Surface Finish;
   a. All external metal finish not covered by soldermask shall be plated 118 - 250 microinches of Electroless Nickel and 2 - 8 microinches of Immersion Gold (ENIG).
5. Via;
   ~~a. All non test point top side vias to be encroached (hole size -5 mils) with soldermask.~~
   ~~b. All non test point bottom side vias to be encroached (hole size +5 mils) and post plug after ENIG process.~~
   ~~c. All via at the BGA device type to be plugged on the same side as the devices are mounted.~~
   d. All bottom BGA vias & test points vias are to be free of soldermask.
   e. Tangency is allowed on vias provided tear dropping is applied to the entry of the trace to the pad. All other plated holes shall have a minimum annular ring of .001".
6. Drilling;
   a. All hole symbols may not be shown in the drawing, See Drill chart for details.
   b. Diameters in the drill table are finished hole sizes with +/-0.003" tolerance unless otherwise specified in the drill table.
7. Marking;
   a. Soldermask,photo-imaged liquid polymer on both sides of boards in accordance with IPC-SM-840, Type B, Class 2, over bare copper, Soldermask color to be Blue.
   b. Component Marking: Silkscreen both sides with white, non-conductive epoxy ink. Lands and exposed plated areas to be free of ink.
   c. Identification: Fab vendor logo and part number with current revision to be etched on the both side. Silkscreen date code on solder side near part number.

UNLESS OTHERWISE SPECIFIED	SIGNATURES	DATE
DIMENSIONS ARE IN INCHES	DRAWN RAJ	02/27/12
TOLERANCES ON:	CHECKED JIM	02/27/12
2 PL DECIMALS +/- .01	ENGRG JIM	02/27/12
3 PL DECIMALS +/- .005	ISSUED	
ANGLES +/- 5°		

Google

FAB DRAWING
SERVO-V2

SIZE	FSCM NO	DWG NO	REV
D		180-10010	04
SCALE NONE		SHEET	1 of 1